Porting NetBSD® to the

RISC-V

"Of course it runs NetBSD!"

Zachary McGrew, Philip A. Nelson

Today's Talk

- Introduction
- Simulators, Toolchains, and Build Scripts, Oh My!
- Moving Targets
- Virtual Memory
- Pmap Common
- Current Status
- Future Work

Introduction - NetBSD

- Free
- Fast
- Secure
- Highly portable
 Unix-like Open
 Source operating
 system



Introduction - NetBSD

- The NetBSD project was started in 1993
 - Happy 25th birthday!
- Zach McGrew is a new NetBSD developer
 - I worked on the RISC-V port for grad school
- Phil Nelson is **Net**BSD developer #6
 - He did the PC532 port
 - Currently updating the Wi-Fi stack
- Runs on **57** different platforms
 - And 16 different types of CPUs
- "Of course it runs NetBSD!"





Introduction - RISC-V

- Originally developed at U.C. Berkeley in 2010 as a teaching example
- A free and open source ISA
- Royalty free too!
- Currently controlled by the RISC-V foundation

• Who are the foundation members?

RISC-V

Google Qualconn

Western Digital.

Ø S E A G A T E









TESLA

HITACHI Inspire the Next



Hewlett Packard Enterprise



Introduction - RISC-V

- Multiple specifications
 - RISC-V ISA
 - RV32I
 - RV32E
 - RV64I
 - RV128I (Seriously)
 - Many extensions to the specification
 - > Privileged ISA

- NetBSD port targets RV64GSU (RV64IMAFDSU)
 - Plans for eventual RV32GSU support

RISC-V

RISC-V Extensions

- A Atomic Instructions
- B Extended Bit Manipulation
- C Compressed Instructions
- D Double-Precision Floating-Point
- E Base Integer Instruction Set (embedded), 32-bit, 16 registers
- F Single-Precision Floating-Point
- G Shorthand for IMAFD extensions
- I Base Integer Instruction Set, [32-bit, 64-bit, or 128-bit], 32 registers
- J Dynamically Translated Languages
- L Decimal Floating-Point
- M Integer Multiplication and Division
- N User-Level Interrupts
- P Packed-SIMD Instructions
- Q Quad-Precision Floating-Point
- **S** Supervisor mode
- T Transactional Memory
- U User mode
- V Vector Operations
- Yxxx/Zxxx Nonstandard vendor extensions

RISC-V

Simulators, Toolchains, and Build Scripts, Oh My!

Simulators

• Spike

- "RISC-V ISA Simulator, implements a functional model of one or more RISC-V processors."
- Feed it a RISC-V binary and run code on your standard AMD64 desktop/laptop
- Spike doesn't have a BIOS/UEFI services
 - Needs a boot loader to actually load the binary (BBL)
 - BBL provides BIOS/UEFI services via SBI
 - BBL probes the hardware and generates the FDT

- Still a problem...
 - Need to build the RISC-V binaries
 - BBL
 - NetBSD Kernel

Toolchains

- BBL needs needs a C library to do some of its work
 - riscv64-unknown-elf-*
 - Build Binutils (gas, Id, and friends)
 - Build GCC
 - Build Newlib (Small C library)
 - Build GCC again

- NetBSD kernel uses it own "mini" C library
 - riscv64--netbsd-*
 - Build Binutils (gas, ld, and friends)
 - Build GCC

Buildscripts

- Building toolchains is complicated, and takes a lot of work
 - You need to pass the correct flags to the configure script
 - Enjoy a sample of my nightmare

- Got a working compiler?
 - o Great
 - Now try and compile the kernel
 - Use the NetBSD build script...

	DINULICI-NEWLID() (
	<pre>cd "\${TOP}/riscv-gnu-toolchain/riscv-binutils-gdb"</pre>
	rm -rf build-binutils
	mkdir build-binutils
	cd huild-hinutils
	#disable-adb
	(configure)
	target_riscu64 unknown olf)
	Larget=riscv64-unknown-eti
	with-arch=rv64imard \
	with-abl=Lp64d \
	prefix=\${RISCV} \
	with-guile=no \
	disable-sim \
	enable-tls \
	disable-intl 🔪
	disable-werror &&
	gmake \${MAKES} && gmake \${MAKES} install
	<pre>gcc-noheaders() {</pre>
	cd "\${TOP}/riscy-onu-toolchain/riscy-occ" &&
	rm -rf huild-occ &&
	mkdir huild acc SS
	ed build acc ff
	(configure)
	/configure (
	Largel=riscv64nelbsd \
	With-arch=rV641matd \
	with-abi=lp64d
	prefix=\${RISCV} \
	without-headers \
	disable-multilib \
	disable-werror \
	disable-shared \
	enable-static 🔪
	disable-threads \
	enable-tls \
	enable-languages=c,c++ \
	disable-libatomic \
	disable-libmudflap
	disable-libssp \
	disable-libquadmath \
	disable-libgomn \
	disable_nls_&
	echo "Preparing to call gmake " &&
	amaka \$/MAKES} all.acc &&
	ache "Bronaring to install acc in CDISCV" SS
	echo Freparing to instatt get in skiste wa
115	gillake ştrakes; instatt-yec
112	U
	gcc-stager() {
	cu stiopy/riscv-gnu-tootchain/riscv-gcc"
	rm -rr build-gcc
	mkair build-gcc
	cd build-gcc
	/configure \
	target=riscv64-unknown-elf \
	with-arch=rv64imafd \
	with-abi=lp64d \
	prefix=\${RISCV} \

Buildscripts - build.sh

- NetBSD uses a build script to wrap its makefiles
 - 1. Build Make without a makefile
 - 2. Do a bunch of automagic detecting of things that Make can't detect
 - 3. Invoke the newly built Make telling it about all the things you've learned
 - 4. Make builds all the tools it needs to build NetBSD
 - 4.1. Uh... We've got our own external toolchain already (fsck!)
 - 4.2. Modify the makefiles to accept an external toolchain
 - 4.3. Rejoice!
 - 5. Make builds the kernel
 - 5.1. Discover ~50 compilation errors in code that's not even in your part of the source tree because you're using a newer, "smarter" version of GCC than the rest of the NetBSD developers
 - 5.2. Turn off -werror
 - 5.3. Rejoice!

Oh My!

- Got a built kernel?
 - Can't load it into Spike directly
- Wrap kernel in BBL
- Each new kernel build requires a build of BBL as well
- Extend build script to automate this process
- Load BBL that holds the kernel into Spike
- Crash & Burn.



Moving Targets

- RISC-V port was started by Matt Thomas in 2015
- Specs weren't as concrete as they are today
 - Specs have changed
 - A lot
 - In small ways
 - But enough to break things everything

• SFENCE.VM Vs. SFENCE.VMA

- One letter difference (Goodbye SFENCE.VM)
- Assembler will still generate opcode for you
- Spike will get angry and crash though...

Moving Targets

- Privileged Spec changed the most
 - Page Table Entries (PTEs) completely redone
 - New way of marking transient entries in page tables
 - Interrupts handled completely different
 - Control and Status registers moved bits all over the place
 - Privileges themselves are mapped differently
 - (Currently) no hypervisor mode May come back?
 - Supervisor can't read user's memory by default
 - Meltdown isn't (currently) a problem on RISC-V! w00t!

Moving Targets

- What does it all mean?
 - locore.S is pretty much garbage at this point
 - Needs a rewrite
 - Start with bootstrapping virtual memory

- RISC-V has three different sizes of virtual memory
 - Sv32 4 GB max memory
 - Sv39 512 GB max memory
 - Sv48 256 TB max memory
- NetBSD port uses Sv39
 - Shouldn't be hard to move to Sv48 in the future, just add extra page of lookups

• Sv39 is three layers

- 512 entries of 1 GB
- 512 entries of 2 MB
- 512 entries of 4 K

- NetBSD takes advantage of the hardware support for big pages
 - Kernel is initially mapped on 2 MB pages
 - Expands on standard 4 K pages when it requests more memory
- Create L1 page table
 - Put entry in for start of kernel address
 - Currently 0xfffffff000000 Makes the math easy
- Create L2 page table
 - Put entries for all 2 MB pages up until just past the end of the kernel
- No L3 pages created by default

- Got a page table? Great!
- Load it into the Supervisor Address Translation and Protection (satp) register
- Crash & Burn.



- Anytime the satp register is changed it causes a fault
- Clever fix (*Thanks FreeBSD*!)
 - Set fault vector to my current address in highmem + 4
 - Set satp
 - Fault to highmem and keep running
 - Set fault vector to real fault handler
- Alternate fix
 - Set bit in mtvec to not fault when satp register changes
 - Requires modifying BBL
 - Repercussions?

- Now running where we belong in virtual memory!
 - Spend and hour writing a console device driver and keep going

•••

Pmap

- Physical mapping of memory in processes
- pmap(9)
 - "machine-dependent portion of the virtual memory system."
- Very complex code
 - FreeBSD RISC-V devs said it was the hardest part of the port for them
- Can't mess it up, or you're in for a world of hurt when debugging

• Every machine does the more or less the same task, why not abstract it further?

Pmap Common

- Started in ~2011 by Matt Thomas Same guy who started RISC-V port
- Handle all the normal work (*machine independent*) that all platforms do anyway
- Call helper functions to do small amounts of *machine dependent* work
- Awesome idea for portability!
- In use by MIPS and (some) PowerPC ports
- Work started to convert other ports to it as well

Pmap Common

- Just one small problem...
 - Only works on platforms without hardware page tables
 - RISC-V has a hardware page table
 - MIPS and PowerPC just have TLBs
 - RISC-V doesn't allow direct writes to the TLB
 - TLB writes are managed by the MMU
- Crash & Burn.



Pmap Common

- This project extended pmap common to support hardware page tables
 - New set of helper functions
 - Create/update hardware specific page tables
 - Do manual lookups when needed
 - Extract hardware bits for permissions

- Some things can't exist in pmap common
 - pmap_bootstrap()
 - Hyper specific to the platform it's running on

Current Status

- Virtual memory
- 🙄 Console driver
- 🙂 Pmap
- white the second second
- fork1()
- cpu_switchto()
- **O** Root file system

Current Status

"Of course it runs NetBSD!"

🖬 1 2 3 4 💽 zmcgrew@nothingman		[Mem: 14%][CPU: 12%][Thermal: 45°C][38][100%] 📶 💲 🔓 🗫 Thu Oct 25, 21:33 📕
zmcgrew@wanderingstar	× zmcgrew@nothingman	× zmcgrew@mrmagpie	e
<pre>memory@80000000 { device_type = "memory"; reg = <0x00000000 0x80000000 0x00000000 }</pre>	0x80000000>;		
<pre>soc { #address-cells = <0x00000002>; #size-cells = <0x00000002>; compatible = "ucbbar,spike-bare-soc", "s compatible = "ucbbar,spike-bare-soc", "s</pre>	imple-bus";		
<pre>ranges; } htif { compatible = "ucb,htif0"; }</pre>			
} entry point set			
0×000000080200000			
entering supervisor mode	00000)		
[1.0000000] pmap steal memory: need 8359	pages		
<pre>[1.0000000] pmap_steal_memory: seg 0: 0x8 [1.00000000] pmap_steal_memory: seg 0: 0x8 [1.00000000] Copyright (c) 1996, 1997, 199 [1.00000000] 2006, 2007, 2008, 2009, 2 [1.0000000] 2018 The NetBSD Foundatio [1.0000000] Copyright (c) 1982, 1986, 198 [1.0000000] The Regents of the Univer</pre>	9395 9800 0x80800 0xc0000 0xc0000 9 pages stolen (0x3d759 left) 8, 1999, 2000, 2001, 2002, 2003, 2004 010, 2011, 2012, 2013, 2014, 2015, 20 n, Inc. All rights reserved. 9, 1991, 1993 sity of California. All rights reser	, 2005, 16, 2017, ved.	
[1.0000000] NetBSD 8.99.25 (GENERIC) #451	: Thu Oct 25 21:22:26 PDT 2018		
[1.00000000] zmcgrew@nothingman:/home/zmc [1.00000000] total memory = 1024 MB [1.00000000] avail memory = 983 MB	grew/netbsd/rv64/obj/sys/arch/riscv/c	ompile/GENERIC	1.1
[1.0000000] mainbus0 (root)cpu0 at mainbu [1.0000000] mainbus0: WARNING: power mana [1.0000030] root on md0a dumps on md0b	s0 instance 0cpu0: WARNING: power man gement not supported	agement not supported	
[1.0000030] Supported file systems: mfs l 0 coda	fs ext2fs ffs nfs umap procfs overlay	null kernfs fdesc union tmpfs smbfs	puffs ptyfs ntfs msdos cd966
<pre>[1.0000030] no file system for md0 (dev 0 [1.0000030] cannot mount root, error = 79 [1.0000030] root device (default md0a);</pre>	x12e00)		
[0] 0:spike* 1:bash- 2:bash 3:bash 4:bash	5:less 6:bash		"nothingman" 21:30 25-Oct-18

Current Status

- I joined the NetBSD Project and got my commit bit last month
- Maya got userland built, so I'll be at the hacker lounge tonight trying to get it running the init process.
- Need some free time to sit down and work with Maxime Villard (port maintainer) and get it merged into the CVS tree
 - Side note: I graduated and got a job with weekends off, so this can actually happen =)

- BCCOTT.COCOpT.cBeidtion to esto Buildesto Bu
 - Othreendby/bebipgns/antkealdynpbay/MgtthidwRGBeenV code
 - Ennated teto stop slacking and keep working
 - Getting rid of the external toolchains
 - Ability to build a root file system
 - Hey who likes userland tools?

- Other simulators
 - QEMU seems to be popular among RISC-V community

- Booting on physical hardware
 - SiFive HiFive Unleashed board is sitting on my workbench
 - Get access to devices Like networking!

• DDB

- Stack traces on RISC-V are weird
- RISC-V has a return address register (ra)
- This means the return address doesn't always get pushed onto the stack
 - Provides a speedup by not doing this, but makes it harder to debug
- Started work on this, but haven't figured out a way to extract the needed information
- Current debugging method: printf();

• FDT support

- Would be nice to know exactly what the hardware is
- Also memory ranges
 - System currently makes assumption about RAM

• SMP

- Machines have all these "extra" cores now...
- Might as well use them?
 - Currently all cores besides the first just sit in an infinite loop waiting on interrupts
- Requires IPI work and probably more locking

• RV32 compatibility

- **Net**BSD has extensive compatibility for other platforms
 - AMD64 can run i386 binaries
 - Aarch64 can run arm32 binaries
 - Would be neat if RV64 could run RV32 binaries

- Reclaim wasted memory after kernel and up to 2 MB boundary
 - Non-debug kernel is slightly over 8 MB, which means 10 MB gets mapped
 - Rest of that space can't be reclaimed
 - What's the fix?
 - Map 8 MB on 2 MB pages, then the rest on 4 K pages

- Teach malloc() about big pages
 - Could help speed up memory requests for memory hungry programs
 - Looking at you, Firefox.
 - Future research project?

- Move to Sv48 Virtual Memory
 - Expands address space, allowing address space randomisation even more space to play with
 - Shouldn't bee too much work to extend Sv39
 - Kernel option to pick?

Thanks

• Phil Nelson - Research advisor and all around awesome dude

• Aran Clauson - For inspiration and listening to my dumb ideas

• Nick Hudson - Helped with PMAP Common stuff when I was really lost

• Matt Thomas - Starting PMAP Common and RISC-V port

